# Shenzhen Leadtek Electronics Co.,Ltd

## PRODUCT SPECIFICATION

## TFT-LCD MODULE

**Module No：** LTK013QVBLM02-V1

☑ Preliminary Specification

☐ Approval Specification

| Designed by | Checked by | Approved by |
|---|---|---|
|  |  |  |

**Final Approval by Customer**

| Approved by | Comment |
|---|---|
| | |

※The specification of “TBD” should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.

# Contents

# 1.Document Revision History

| Version | Contents | Date | Note |
|---|---|---|---|
| V0 | Original | 2022.04.25 | |
| V1 | The backlit plastic frame material is changed to black material,<br>and the FPC is brushed with black oil | 2022.05.26 | |
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# 2. Introduction

## 2.1 Scope of application

This specification applies to the LCD module that is supplied by Shenzhen Leadtek Electronics Co.,Ltd
LCD specification: Dots 240xRGBx240.
As to basic specification of the driver IC, refer to the IC (ST7789V2) specification and data book.
All material & processing of the LCD module should be Lead Free.

## 2.2 TFT features:

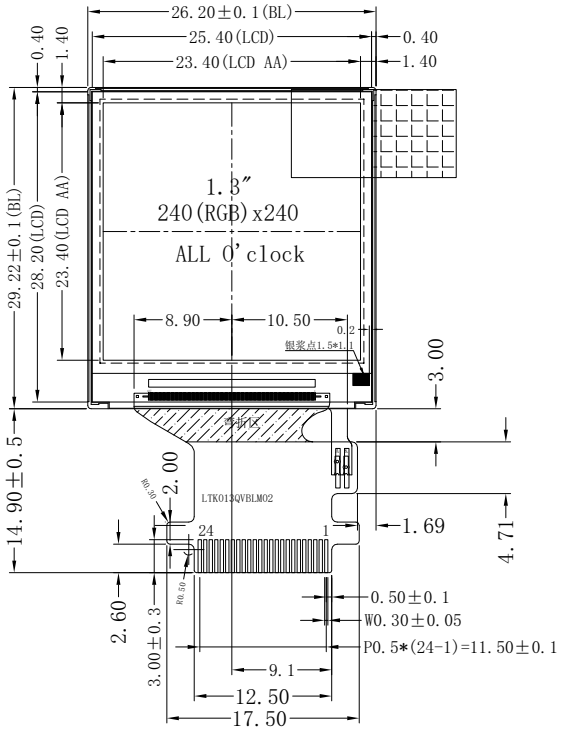
Structure:  TFT PANNEL+IC +FPC+BL;
IPS Type LCD
240dot-segment and 240 dot-common outputs;
262K Color can be selected by software;
White LED back light;
4line SPI &8bit MCU interface

## 2.3 Applications:

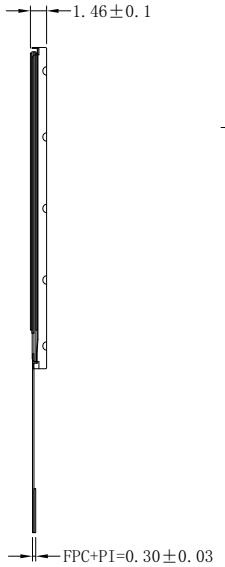
## 3. LCM General specification

| ITEM | Sandard value | Unit |
|---|---|---|
| LCD Type | Normally black | -- |
| Drive element | TFT active matrix | -- |
| Number of pixels | 240(H) RGB × 240(V) | Dots |
| Pixel arrangement | RGB Vertical Stripe | -- |
| Pixel Pitch (H*V) | 0.0975(H) × 0.0975(V) | mm |
| Active area | 23.40(H) × 23.40(V) | mm |
| Viewing direction | ALL O'CLOCK | - |
| TFT Driver IC | ST7789V2 | |
| TFT interface | 4line SPI&8bit MCU interface | - |
| Approx. Weight | TBD | g |
| LCM Size(W*H*T) | 26.20(W) ×29.22(H) ×1.46(T) | mm |

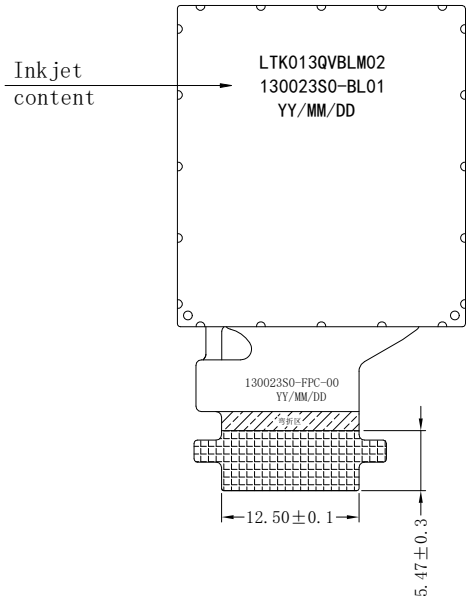
# Front View




# Side View

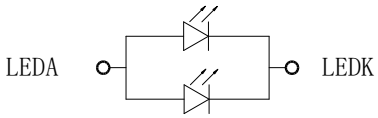



# Back View




FPC launches shipment

| Pin | Assignment |
|---|---|
| 1 | LEDA |
| 2 | LEDK |
| 3 | GND |
| 4 | VDD |
| 5 | VDDIO |
| 6 | IM1/2 |
| 7 | RESET |
| 8 | CS |
| 9 | D/C SCK |
| 10 | WR SDC |
| 11 | RD |
| 12 | SDA |
| 13 | DB0 |
| 14 | DB1 |
| 15 | DB2 |
| 16 | DB3 |
| 17 | DB4 |
| 18 | DB5 |
| 19 | DB6 |
| 20 | DB7 |
| 21 | TE |
| 22 | NC |
| 23 | GND |
| 24 | GND |




IM1/2=1 4-SPI
IM1/2=0 80-8BIT

NOTES:
1. DISPLAY TYPE: 1.3″, 240*240 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL O'clock
4. DRIVER IC:ST7789V2
5. LCM (White 9 AVG 1/9) :
   Brightness: 1000 cd/m² (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 2 chip white LEDs If=40mA,Vf=5.6V-6.4V
7. OPERATING TEMP: -20° C TO 60° C,STORAGE TEMP: -30° C TO 70° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

| REV | DESCRIPTION | DATE | NAME |
|---|---|---|---|
| 2 | | | |
| 1 | The backlit plastic frame material is changed to black material, and the FPC is brushed with black oil | 2022.05.26 | Ian |
| 0 | NEW | 2022.03.23 | Ian |

LEADTEK COMPANY LIMITED

| SCALE:1/1 | UNIT:mm | PAGE:1/1 | | Approve | Check | Drawn |
|---|---|---|---|---|---|---|
| Part No: | LTK013QVBLM02 | | VER:V1 | | | |
| Customer No: | | | | | steven | Ian |

# 4.Absolute Maximum Rating

| Characteristics | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| LCM Operating Temperature | $T_{OPR}$ | -20 | +60 | °C |
| LCM Storage Temperature | $T_{STG}$ | -30 | +70 | °C |
| Humidity | RH | - | 90 | % |

# 5.Electrical Characteristics

## 5.1 TFT DC Characteristics

| Characteristics | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Supply Voltage for I/O | VDDIO | 1.65 | 1.8 | 3.3 | V | |
| Supply Voltage for(DC/DC) | VDD | 2.5 | 2.8 | 3.3 | V | |
| TFT Gate ON Voltage | VGH | 12 | -- | 18 | V | *1,*2 |
| TFT Gate OFF Voltage | VGL | -10 | -- | -7 | V | *1,*2 |
| TFT Common Voltage | Vcom | -2 | -- | 5 | V | *3 |

Note:

*1. VGH is TFT Gate operating Voltage.

*2. VGL is TFT Gate operating Voltage.

The storage structure of this model is $C_{ST}$(Storage on Common)

*3. Vcom must be adjusted to optimize display quality _Cross talk, Contrast Ratio and etc.

## 5.2 Back-Light Unit Characeristics

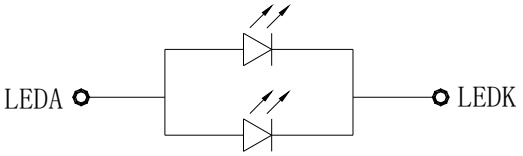
The back-light system is an edge-lighting type with white 2 LEDs. The characteristics of the back-light are shown in the following tables.

| Characteristics | Symbol | Min. | Type | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_F$ | 5.6 | -- | 6.4V | | - |
| Forward current | $I_F$ | -- | 40 | -- | mA | - |
| Luminance(With LCD) | Lv | | 1000 | | $cd/m^2$ | - |
| LED life time | N/A | -- | 20,000 | -- | Hr | Note 1 |

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at $I_L$=20mA/LED. The LED life time could be decreased if operating $I_L$ is larger than 25mA/LED.

Backlight circuit diagram shown in below:



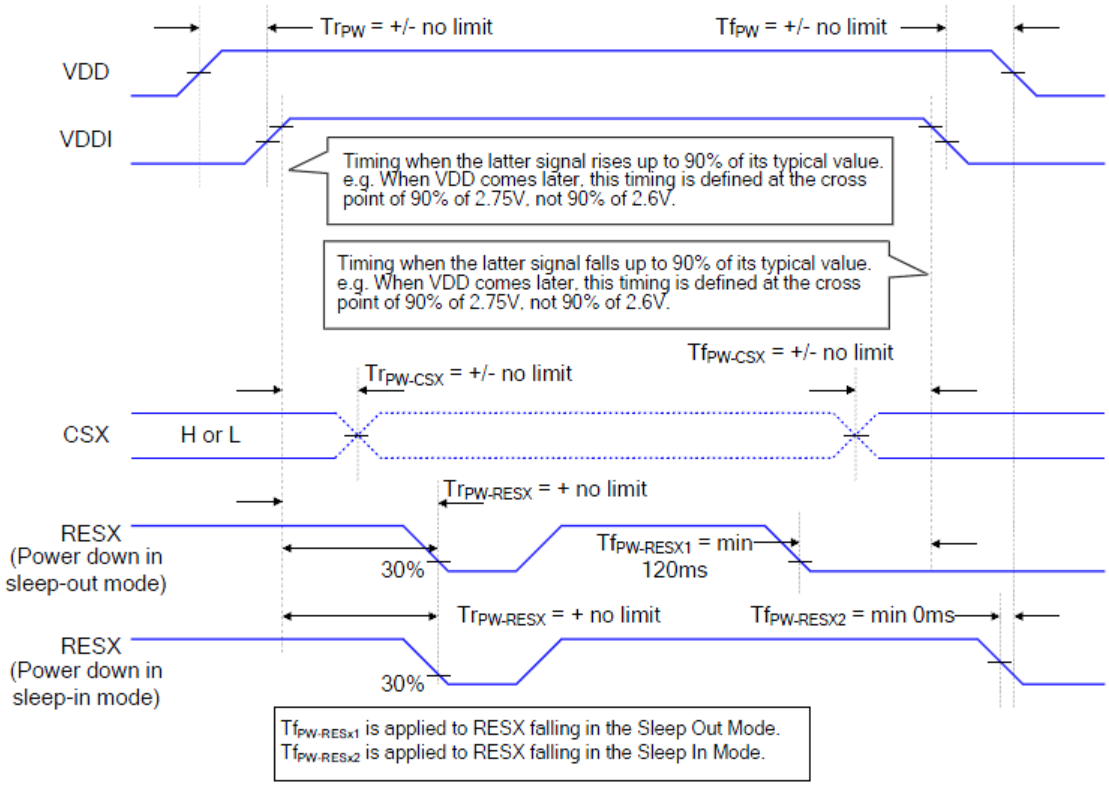

## 6. Module Function Description

| Pin No. | Symbol | LCM Description | remarks |
|---|---|---|---|
| 1 | LEDA | Power Supply For LED Backlight Anode Input. | |
| 2 | LEDK | Power Supply For LED Backlight Anode Input. | |
| 3 | GND | Ground | |
| 4 | VDD2.8V | Power Supply For LCD.(2.5-3.3V) | |
| 5 | VDDIO1.8V | Power Supply For I/O.(1.65-3.3V) | |
| 6 | IM1/2 | The MCU interface mode select | |
| 7 | RESET | Global reset pin | |
| 8 | CS | Chip select signal input pin | |
| 9 | D/C_SCK | Serial clock signal. | |
| 10 | WR_SDC | Write strobe signal. | |
| 11 | RD | Read strobe signal. | |
| 12 | SDA | input/output signal pin | |
| 13~20 | DB0~DB7 | MCU parallel interface data bus. | |
| 21 | TE | Frame head pulse for tearing effect. | |
| 22 | NC | NC | |
| 23~24 | GND | Ground | |

# 7. Timing Characteristics

## Power ON/OFF Sequence

The power on/off sequence is illustrated below



**8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus:**

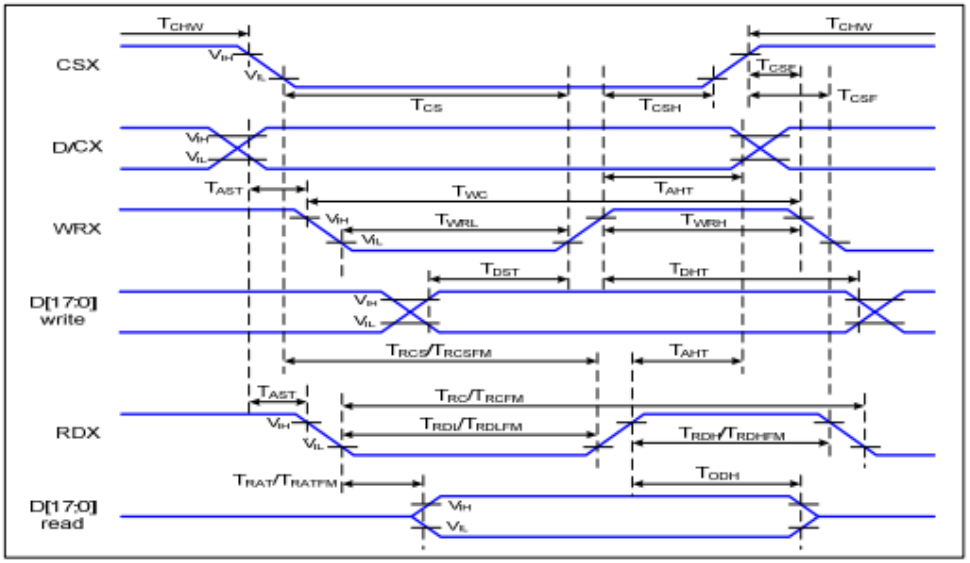



**Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)**

*VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃*

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|---|---|---|---|---|---|---|
| D/CX | $T_{AST}$ | Address setup time | 0 | | ns | - |
| | $T_{AHT}$ | Address hold time (Write/Read) | 10 | | ns | |
| CSX | $T_{CHW}$ | Chip select "H" pulse width | 0 | | ns | - |
| | $T_{CS}$ | Chip select setup time (Write) | 15 | | ns | |
| | $T_{RCS}$ | Chip select setup time (Read ID) | 45 | | ns | |
| | $T_{RCSFM}$ | Chip select setup time (Read FM) | 355 | | ns | |
| | $T_{CSF}$ | Chip select wait time (Write/Read) | 10 | | ns | |
| | $T_{CSH}$ | Chip select hold time | 10 | | ns | |
| WRX | $T_{WC}$ | Write cycle | 66 | | ns | |
| | $T_{WRH}$ | Control pulse "H" duration | 15 | | ns | |
| | $T_{WRL}$ | Control pulse "L" duration | 15 | | ns | |
| RDX (ID) | $T_{RC}$ | Read cycle (ID) | 160 | | ns | When read ID data |
| | $T_{RDH}$ | Control pulse "H" duration (ID) | 90 | | ns | |
| | $T_{RDL}$ | Control pulse "L" duration (ID) | 45 | | ns | |
| RDX (FM) | $T_{RCFM}$ | Read cycle (FM) | 450 | | ns | When read from frame memory |
| | $T_{RDHFM}$ | Control pulse "H" duration (FM) | 90 | | ns | |
| | $T_{RDLFM}$ | Control pulse "L" duration (FM) | 355 | | ns | |
| D[17:0] | $T_{DST}$ | Data setup time | 10 | | ns | For CL=30pF |

**8080 Serial Interface Characteristics (4-line serial):**

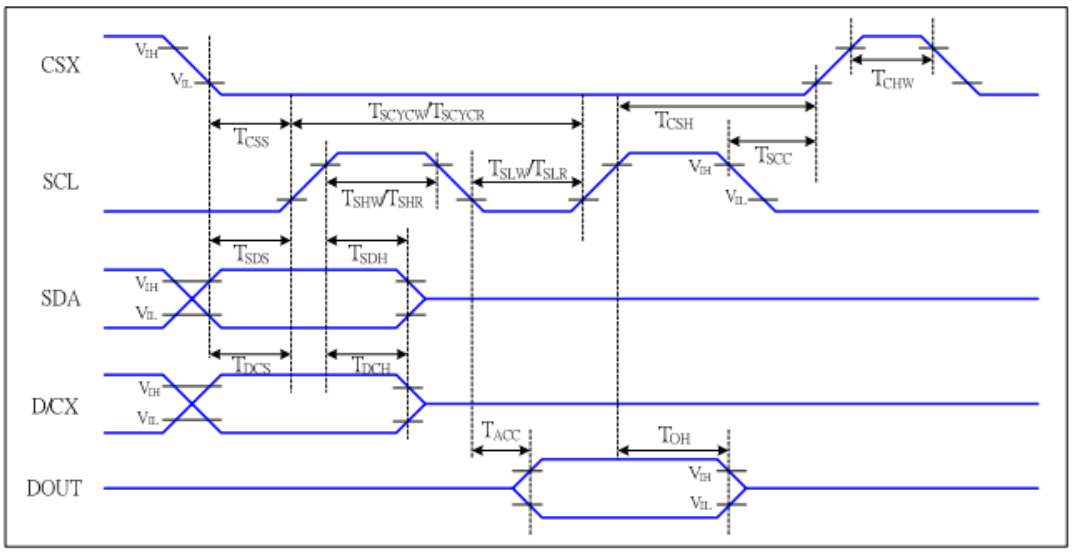



**Figure 5 4-line serial Interface Timing Characteristics**

*VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃*

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | $T_{CSS}$ | Chip select setup time (write) | 15 | | ns | |
| | $T_{CSH}$ | Chip select hold time (write) | 15 | | ns | |
| | $T_{CSS}$ | Chip select setup time (read) | 60 | | ns | |
| | $T_{SCC}$ | Chip select hold time (read) | 65 | | ns | |
| | $T_{CHW}$ | Chip select "H" pulse width | 40 | | ns | |
| SCL | $T_{SCYCW}$ | Serial clock cycle (Write) | 66 | | ns | -write command & data ram |
| | $T_{SHW}$ | SCL "H" pulse width (Write) | 15 | | ns | |
| | $T_{SLW}$ | SCL "L" pulse width (Write) | 15 | | ns | |
| | $T_{SCYCR}$ | Serial clock cycle (Read) | 150 | | ns | -read command & data ram |
| | $T_{SHR}$ | SCL "H" pulse width (Read) | 60 | | ns | |
| | $T_{SLR}$ | SCL "L" pulse width (Read) | 60 | | ns | |
| D/CX | $T_{DCS}$ | D/CX setup time | 10 | | ns | |
| | $T_{DCH}$ | D/CX hold time | 10 | | ns | |
| SDA (DIN) | $T_{SDS}$ | Data setup time | 10 | | ns | |
| | $T_{SDH}$ | Data hold time | 10 | | ns | |
| DOUT | $T_{ACC}$ | Access time | 10 | 50 | ns | For maximum CL=30pF |
| | $T_{OH}$ | Output disable time | 15 | 50 | ns | For minimum CL=8pF |

**Table 6 4-line serial Interface Characteristics**

*Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.*

**Reset Timing:**

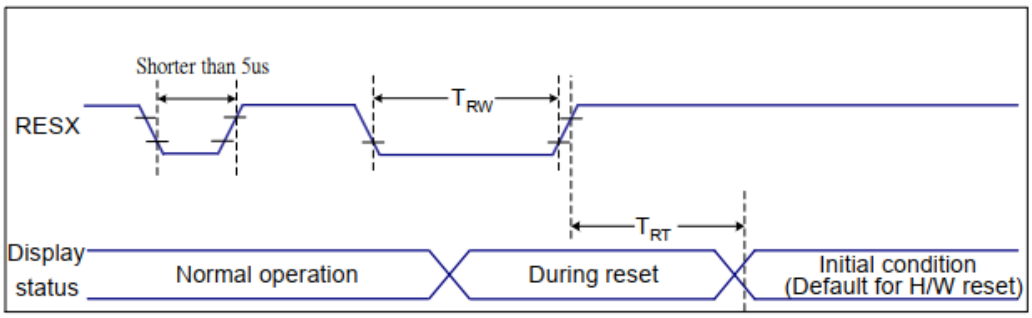



**Figure 7 Reset Timing**

*VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃*

| Related Pins | Symbol | Parameter | MIN | MAX | Unit |
|---|---|---|---|---|---|
| RESX | TRW | Reset pulse duration | 10 | - | us |
| | TRT | Reset cancel | - | 5 (Note 1, 5) | ms |
| | | | | 120 (Note 1, 6, 7) | ms |

**Table 9 Reset Timing**

*Notes:*

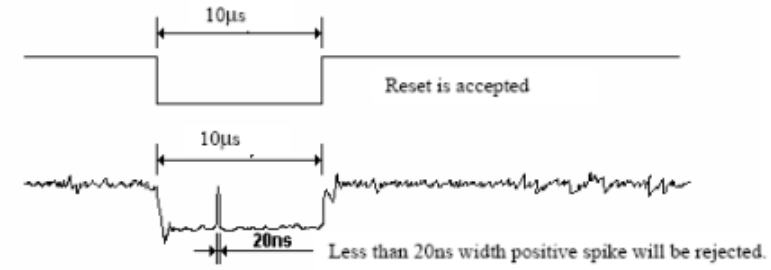
*1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.*

*2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:*

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9us | Reset starts |

*3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.*

*4. Spike Rejection also applies during a valid reset pulse as shown below:*




*5. When Reset applied during Sleep In Mode.*

*6. When Reset applied during Sleep Out Mode.*

*7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.*

## 8.Optical Characteristics

| Parameter | | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| Threshold Voltage | | Vsat | | 4.1 | 4.3 | 4.5 | V | Fig.1 |
| | | Vth | | 1.6 | 1.8 | 2.0 | V | |
| Viewing Angle | Horizontal | Θ3 | CR>10 | 70 | 80 | | ° | Note 1 |
| | | Θ9 | | 70 | 80 | | ° | |
| | Vertical | Θ12 | | 70 | 80 | | ° | |
| | | Θ6 | | 70 | 80 | | ° | |
| Contrast Ratio | | CR | Θ= 0° | 600 | 800 | | | Note 2 |
| Transmittance | | T(%) | Θ= 0° | 4.1 | 4.59 | | | Note 3 |
| NTSC | | % | Θ= 0° | 45 | 50 | | | |
| Reproduction Of color | Red | Rx | Θ= 0° | 0.610 | 0.625 | 0.640 | | Note 4 *Color filter Glass with OC |
| | | Ry | | 0.295 | 0.310 | 0.325 | | |
| | Green | Gx | | 0.280 | 0.295 | 0.310 | | |
| | | Gy | | 0.503 | 0.518 | 0.533 | | |
| | Blue | Bx | | 0.127 | 0.142 | 0.157 | | |
| | | By | | 0.128 | 0.143 | 0.158 | | |
| White | | Wx | Θ= 0° | | TBD | | | |
| | | Wy | | | TBD | | | |
| Response Time | | Tr+Tf | Θ= 0° | | 30 | 35 | ms | Note 5 |

**Note:**

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIG.2).
2. Contrast measurements shall be made at viewing angle of Θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIG. 2) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the value without APF Pol.
4. The color chromaticity coordinates specified in Table1 shall be calculated from The spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the C/F. Measurement condition is C - light source & Halogen Lamp
5. The electro-optical response time measurements shall be made as FIG.3 by switching the "data" input signal ON and OFF.
The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

**Figure 1. The definition of Vth & Vsat**

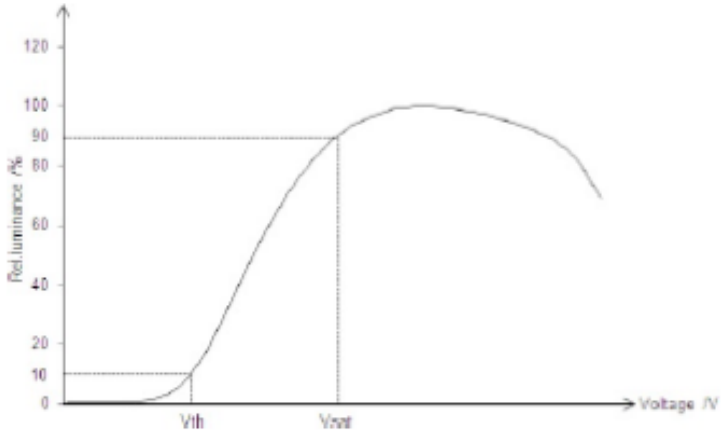



**Figure 2. Measurement Set Up**

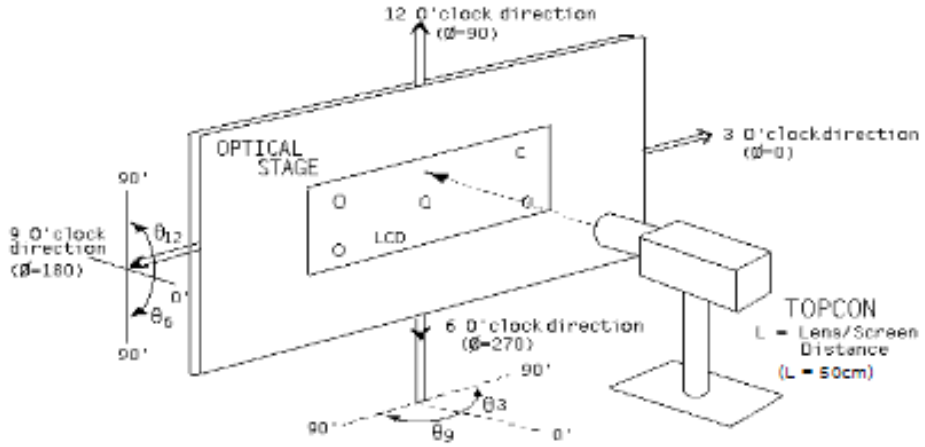
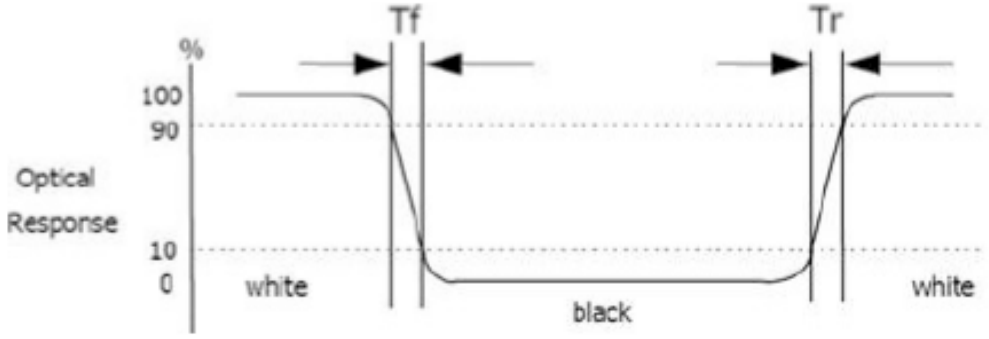



**Figure 3. Response Time Testing**



## 9. Reliability Test Item

| No. | Test Item | Test Condition | Notes |
|---|---|---|---|
| 1 | High Temp. Storage | +70°C / 96H | 1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow. |
| 2 | Low Temp. Storage | -30°C / 96H | |
| 3 | High Tempe. Operating | +60°C / 96H | |
| 4 | Low Tempe. Operating | -20°C / 96H | |
| 5 | High Temperature /Humidity storage | 50°C x 90%RH / 96H | |
| 6 | Thermal and cold shock | Static state，-30℃（30min）~60℃（30min），50 cycles | |

## 10. Packing Method------TBD