

True Multi-Touch Capacitive Touch Panel Controller

INTRODUCTION

The FT5X26 is single-chip capacitive touch panel controllers with built-in enhanced Micro-controller unit (MCU). It provides the benefits of full screen common mode scan technology, fast response time and high level of accuracy. It can drive capacitive type touch panel with up to 35 driving and 21 sensing lines.

FEATURES

- Mutual Capacitive Sensing Techniques
- Full Screen Common Mode Scan Techniques
- True Multi-touch up to 10 Points of absolute X and Y Coordinates
- High immunity to RF and power Interferences
- 5526EEZ Supports up to 35TX + 21 RX
- Full Programmable Scan Sequences to Support Various TX/RX Configurations
- High Report Rate: Over 100Hz
- Touch Resolution of 325 Dots per Inch (dpi) or above
- Auto-calibration
- Support Interfaces: I2C
- Built-in 64KB Flash
- 2.8 to 3.6V Operating Voltage
- IOVCC (Ext. or Int.) supports from 1.8V to 3.6V
- Single Channel (TX/RX) resistance: Up to 100K Ω
- Single Channel (transmit/receive) Capacitance: 20pF
- Optimal Sensing Mutual Capacitor: 0.5pF~4pF
- 12-Bit ADC Accuracy
- 3 Operating Modes
 - Active
 - Monitor
 - Hibernation
- Operating Temperature Range: -40°C to +85°C
- Package:
 - QFN68L 8x8x0.8mm, 0.4mm/pitch

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1 OVERVIEW

1.1 Typical Applications

FT5X26 accommodates a wide range of applications with a set of buttons up to a 2D touch sensing device; their typical applications are listed below.

- Tablets
- Navigation systems, GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras

FT5X26 support Touch Panel, the spec is listed in the following table,

Part Number	Package	TX	RX	Total Channels	Recommended for Tablet TP Size (16:9)
FT5526EEZ	QFN 68L8x8x0.8mm Pitch =0.4mm	35	21	56	≤9", Sensor Pitch:6mm

2 FUNCTIONAL DESCRIPTION

2.1 Architectural Overview

Figure2-1 shows the overall architecture for the FT5X26.

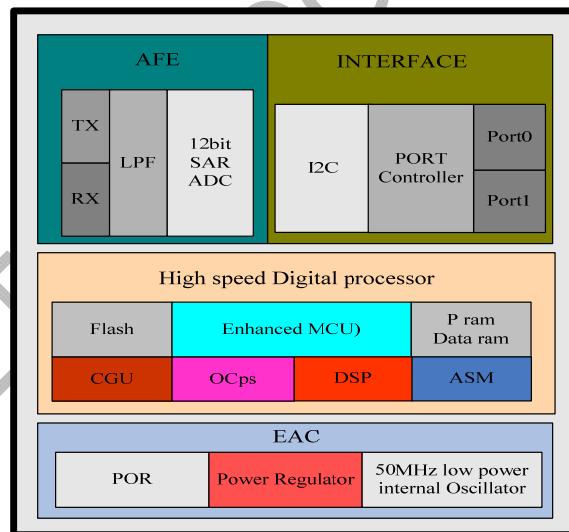


Figure 2-1 System Architecture Diagram

The FT5X26 is comprised of five main functional parts listed below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. It includes both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces.

- Enhanced MCU with DSP accelerator

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash memory is

implemented to store programs and some key parameters.

Complex signal processing algorithms are implemented by MCU and DSP accelerator to detect the touches reliably and efficiently. Communication protocol software is also implemented in this MCU to exchange data and control information with the host processor.

- External Interface
 - I2C: an interface for data exchange with host
 - INT: an interrupt signal to inform the host processor that touch data is ready for read
 - RSTN: an external low signal reset the chip. The port is also use to wake up the FT5X26 from the Hibernate mode.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply
- Power On Reset (POR) is active until VDDD is higher than some level and hold decades of μ s.

2.2 MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- A DSP accelerator cooperates with MCU to process the complex algorithms
- Timer: A number of timers are available to generate different clocks
- Clock Manager: To control various clocks under different operation conditions of the system

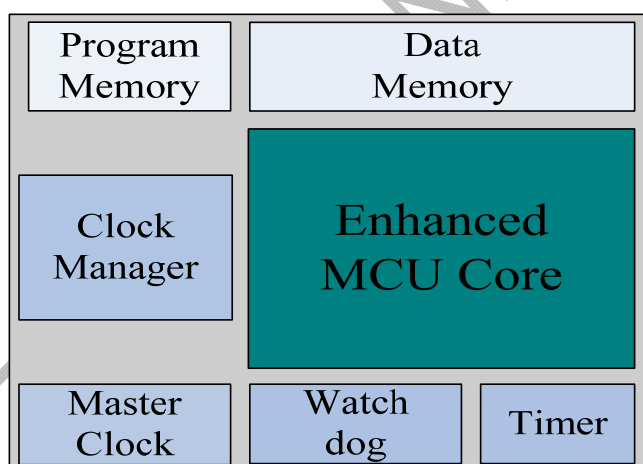


Figure 2-2 MCU Block Diagram

2.3 Operation Modes

FT5X26 offers following three modes:

- **Active Mode**

When in this mode, FT5X26 actively scans the panel. The default scan rate is 100 frames per second. The host processor can configure it to speed up or to slow down.

- **Monitor Mode**

In this mode, FT5X26 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. In this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5X26 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- **Hibernate Mode**

In this mode, the chip is set in a power down mode. It shall only respond to the "RESET" signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.4 Host Interface

Figure 2-3 shows the interface between a host processor and FT5X26. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT5X26 to the Host
- Reset Signal from the Host to FT5X26

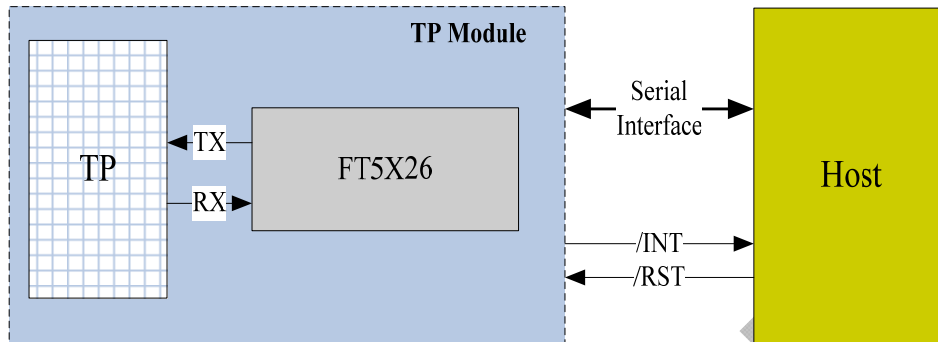


Figure 2-3 Host Interface Diagram

The serial interface of FT5X26 is I2C. The detail of the interface is described in detail in Section 2.5. The interrupt signal (/INT) is used for FT5X26 to inform the host that data are ready for the host to receive. The /RST signal is used for the host to wake up FT5X26 from the Hibernate mode. After resetting, FT5X26 shall enter the Active mode.

2.5 Serial Interface

FT5X26 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4**.

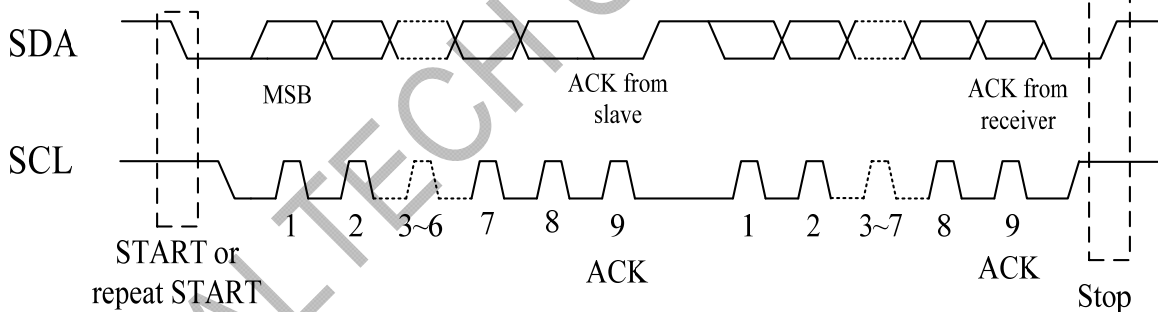


Figure 2-4 I2C Serial Data Transfer Format

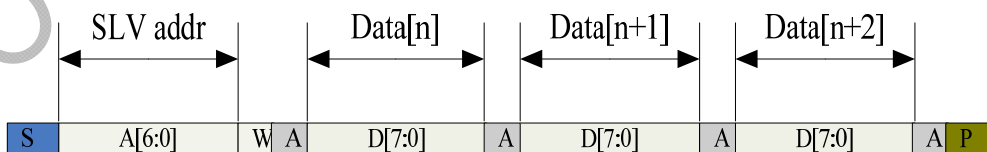


Figure 2-5 I2C master write, slave read

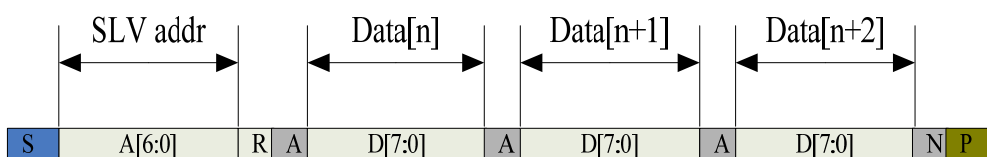


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0' for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7		us
Hold time (repeated) START condition	4.0		us
Data setup time	250		ns
Setup time for a repeated START condition	4.7		us
Setup Time for STOP condition	4.0		us

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage 1	VDDA - VSSA	-0.3 ~ +3.6	V	1, 2
Power Supply Voltage 2	VDD3 - VSS	-0.3 ~ +3.6	V	1, 3
I/O Digital Voltage	IOVCC	1.8~3.6	V	1
Operating Temperature	Topr	-40 ~ +85	°C	1
Storage Temperature	Tstg	-55 ~ +150	°C	1

Notes

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1. If used beyond the absolute maximum ratings, FT5X26 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDDA (high) \geq VSSA (low)
3. Make sure VDD (high) \geq VSS (low)

3.2 DC Characteristics

Table 3-2 DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V	IOH=-0.1mA	0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V	IOH=0.1mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	uA	Vin=0~VDDA	-1	--	1	
Current consumption (Normal operation mode)	Iopr	mA	VDDA=VDD3 = 2.8V Ta=25°C MCLK=24MHz	--	11.00	--	
Current consumption (Monitor mode)	Imon	mA	VDDA=VDD3 = 2.8V Ta=25°C MCLK=24MHz	--	0.87	--	
Current consumption (Sleep mode)	Islp	uA	VDDA=VDD3 = 2.8V Ta=25°C MCLK=24MHz	--	78.8	--	
Step-up output voltage	VDD5	V	VDDA=VDD3= 2.8V		0.25		
Power Supply voltage	VDDA VDD3	V		2.8	--	3.6	

Notes: This consumption data is intended for design guidance only. Actual current will depend on the particular sensor design and firmware options.

3.3 AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V; Ta=25°C	49	50	51	

Table 3-3 AC Characteristics of TX & RX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		100	150	400	KHz	
TX output rise time	Ttxr		--	TBD	--	nS	
TX output fall time	Ttxf		--	TBD	--	nS	
RX input voltage	Trxi		1.2	TBD	1.6	V	

3.4 I/O Ports Circuits

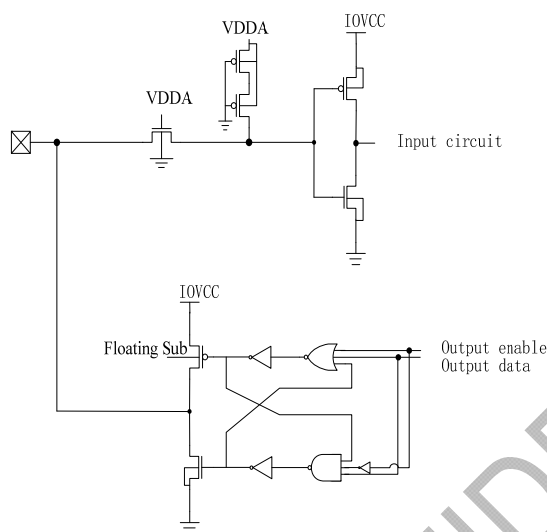


Figure 3-1 General Purpose In/Out Port Circuit.

The input/output property can be configured via firmware setting. The firmware can also control its output behavior as push-pull or as open-drain that SDA of I2C interface is required.

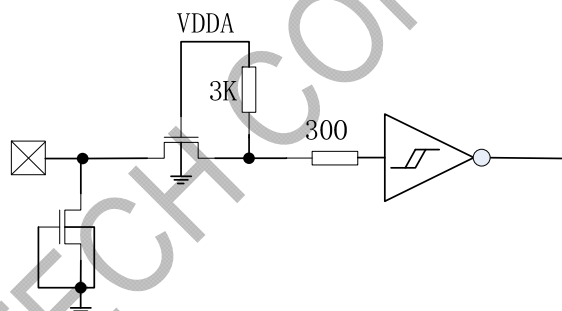


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (T_{rtp}). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and T_{pdt} is more than 1ms.

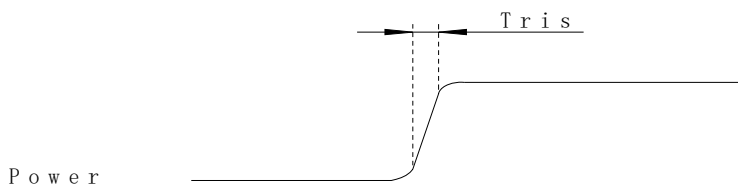


Figure 3-3 Power on time

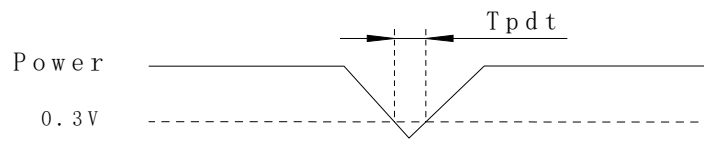


Figure 3-4 Power Cycle requirement

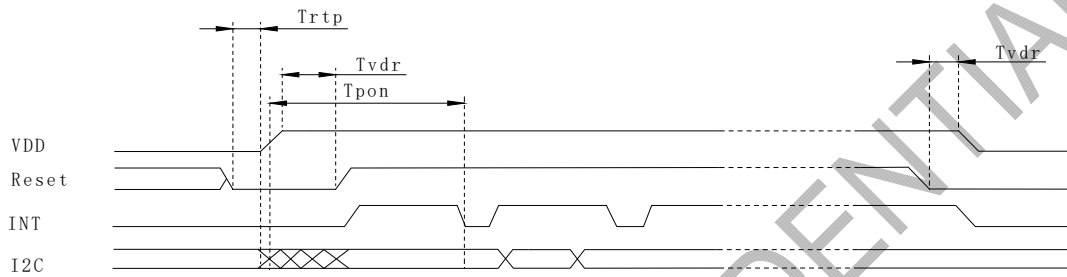


Figure 3-5 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

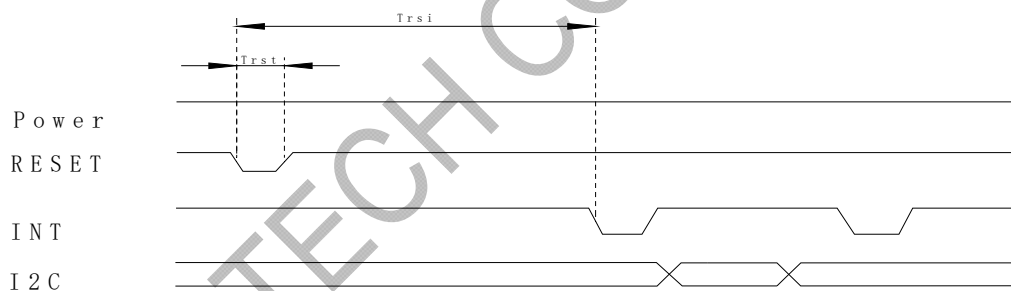


Figure 3-6 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tpon	Time of starting to report point after powering on	200	--	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	200	--	ms
Trst	Reset time	1	--	ms

4 PIN CONFIGURATIONS

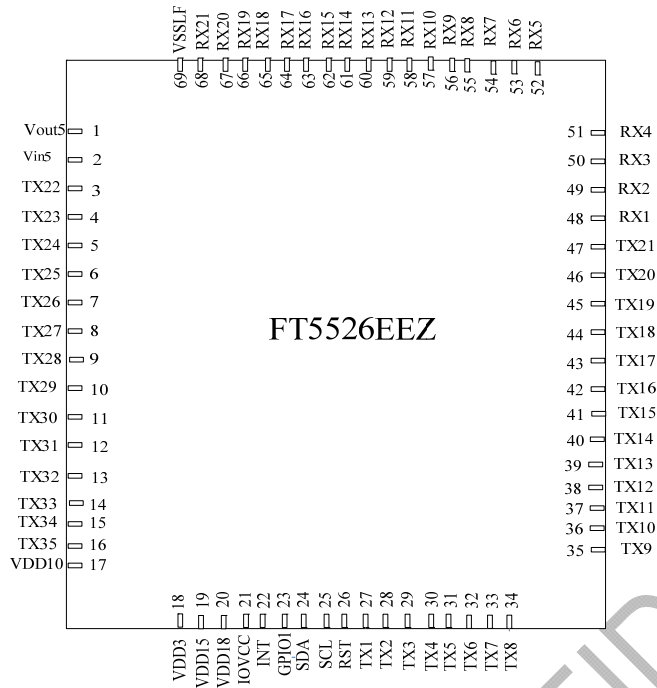
Pin List of FT5X26

Table 4-1 Pin Definition

Name	Pin No.	Type	Description
	FT5526EEZ		
RX21	68	I	Receiver input pins
RX20	67	I	Receiver input pins
RX19	66	I	Receiver input pins
RX18	65	I	Receiver input pins
RX17	64	I	Receiver input pins
RX16	63	I	Receiver input pins
RX15	62	I	Receiver input pins
RX14	61	I	Receiver input pins
RX13	60	I	Receiver input pins
RX12	59	I	Receiver input pins
RX11	58	I	Receiver input pins
RX10	57	I	Receiver input pins
RX9	56	I	Receiver input pins
RX8	55	I	Receiver input pins
RX7	54	I	Receiver input pins
RX6	53	I	Receiver input pins
RX5	52	I	Receiver input pins
RX4	51	I	Receiver input pins
RX3	50	I	Receiver input pins
RX2	49	I	Receiver input pins
RX1	48	I	Receiver input pins
VDD5_IN	1	PWR	internal generated 5V power supply, A 1 μ F ceramic capacitor to ground is required.
VSSLF	69	PWR	Analog ground
VDD5_Out	2	PWR	digital power supply, A 1 μ F ceramic capacitor to ground is required.
NC		NC	
TX10	36	O	Transmit output pin
TX11	37	O	Transmit output pin
TX12	38	O	Transmit output pin
TX13	39	O	Transmit output pin
TX14	40	O	Transmit output pin
TX15	41	O	Transmit output pin
TX16	42	O	Transmit output pin
TX17	43	O	Transmit output pin
TX18	44	O	Transmit output pin
TX19	45	O	Transmit output pin
TX20	46	O	Transmit output pin

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TX21	47	O	Transmit output pin
TX22	3	O	Transmit output pin
TX23	4	O	Transmit output pin
TX24	5	O	Transmit output pin
TX25	6	O	Transmit output pin
TX26	7	O	Transmit output pin
TX27	8	O	Transmit output pin
TX28	9	O	Transmit output pin
TX29	10	O	Transmit output pin
TX30	11	O	Transmit output pin
TX31	12	O	Transmit output pin
TX32	13	O	Transmit output pin
TX33	14	O	Transmit output pin
TX34	15	O	Transmit output pin
TX35	16	O	Transmit output pin
VDD10	17	PWR	digital power supply, A 1 μ F ceramic capacitor to ground is required.
VDD3	18	PWR	digital power supply, A 1 μ F ceramic capacitor to ground is required.
VDD15	19	PWR	digital power supply, A 1 μ F ceramic capacitor to ground is required.
VDD18	20	PWR	digital power supply, A 1 μ F ceramic capacitor to ground is required.
IOVCC	21	PWR	I/O power supply
INT	22	I/O	Interrupt request to the host, or Wakeup request from the host.
GPIO1	23	I/O	
SDA	24	I/O	I2C data input and output
SCL	25	I/O	I2C clock input
RSTN	26	I	External Reset, Low is active
TX1	27	O	Transmit output pin
TX2	28	O	Transmit output pin
TX3	29	O	Transmit output pin
TX4	30	O	Transmit output pin
TX5	31	O	Transmit output pin
TX6	32	O	Transmit output pin
TX7	33	O	Transmit output pin
TX8	34	O	Transmit output pin
TX9	35	O	Transmit output pin



FT5526EEZ Package Diagram

Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.55	0.57
L/F Thickness	A3	0.203 REF		
Lead Width	b	0.15	0.2	0.25
Body Size	X	D		
	Y	E		
Lead Pitch	e	0.4 BSC		
EP Size	X	6.1	6.2	6.3
	Y	6.1	6.2	6.3
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.1		
Co Planarity	ccc	0.08		
Lead Offset	ddd	0.1		
Exposed Pad Offset	eee	0.1		

5.2 Order Information

Package Type	QFN
	68Pin(8 * 8)
	68Pin(0.8 – P0.4)
Product Name	FT5526
<p>Note:</p> <ol style="list-style-type: none"> 1). The last three letters in the product name indicate the package type , lead pitch and thickness and numbers of TX and RX. 2). The third last letter indicates the package type . E : QFN-8*8 3). The second last letter indicates the lead pitch and thickness. E : 0.8 - P0.4 4). The last letter indicates the numbers of TX and RX. Z: 35TX-21RX 	

T: Track Code


F/R: " F" for Lead Free process,
" R" for Halogen Free process

Y: Year Code

WW: Week Code

S: Lot Code

FT 5X26
T F Y W W S V



Product Name	Package Type	# TX Pins	# RX Pins
FT5526EEZ	QFN-68L	35	21

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